Cross-coupled folding circuit and analog-to-digital converter provided with such a folding circuit

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The invention relates to a cross-coupled folding circuit, comprising a reference voltage circuit to supply a series of m reference voltages, an amplifier circuit to provide a series of control signals in response to an input signal and to the reference voltages, and a number of differential transistor pairs in a cascade configuration controlled by said control signals, each differential pair of transistors being active in a voltage range around one of said reference voltages.

Such a cross-coupled folding circuit is known from US-A-6,236,348. Particularly in Fig. 4 of said patent specification a three times folding circuit, i.e. a cascade configuration of successively two and one differential transistor pairs is shown, while in Fig. 9 a seven times folding circuit in a cascade configuration in three successive steps of four, two and one differential transistor pairs, is shown. The differential transistor pairs in the cross-coupled folding circuit of said US patent specification are only controlled by signals, derived from an input signal and a series of reference voltages. A cascade configuration of cross coupled folding circuits, wherein each cross coupled folding circuit of a successive array of cross coupled folding circuits is controlled by output signals of a respective cross coupled folding circuit of a former array is not well possible; this contrary to, for example, a cascade configuration of parallel folding circuits.

The aim of the invention is to obtain a cross-coupled folding circuit in which this restriction is overcome and which has a limited quantity of hardware, a large folding factor and a low energy consumption.

Therefore, according to the invention, the cross-coupled folding circuit as described in the opening paragraph is characterized in that $2^n - 1$ three times cross-coupled folding circuits are provided, each of which comprising three differential pairs of transistors, and, in a cascade configuration with said $2^n - 1$ folding circuits, in n-1 successive steps 2^{n-1}, 2^{n-2}, ..., 2^0 differential transistor pairs, the control signals thereof being supplied by the series